REMARKS

Minor corrections have been made to the specification. The title has been made more descriptive. Claims 1-8 have been canceled, without prejudice. Claims 9-14 have been added. Claims 9-14 remain pending. Reconsideration and reexamination of the application, as amended, are requested.

Applicant acknowledges the election of claims 1-7, without traverse. Claims 1-7 have now been canceled, without prejudice. Claims 9-14 replace claims 1-7 and are within the scope of the election.

The Examiner objected to the title as not being descriptive. The title has been amended to be made more descriptive. It is submitted that the title is acceptable.

The disclosure was objected to because of certain informalities. The informalities have been considered and the specification appropriately amended where necessary. Figure 9 has been amended to include numerals "21" and "82". A marked-up copy of Figure 9 is enclosed for approval.

The Examiner objected to the drawings by indicating that the thinner wiring wire at the irradiated region, as recited in claim 1, was not shown. Claim 1 has been canceled. The new claims do not claim a thinner wiring layer.

The Examiner objected to claims 1-7 because of a misspelling of the word "wiring". It is believed that corrections have been made where necessary.

The Examiner rejected claims 1-4 under 35 U.S.C. § 112, first paragraph. The Examiner indicated that there was no support in the specification for a wiring layer at the irradiated region being thinner than the wiring layer at other regions, as recited in claim 1. This limitation is no longer claimed in the new claims.

The Examiner rejected claims 1-4 under 35 U.S.C. § 112, second paragraph, as being indefinite. The Examiner indicated several phrases as being troublesome. The original claims have been canceled and now replaced with new claims. It is submitted that the new claims are definite.

The Examiner rejected claims 1-7 under 35 U.S.C. § 103(a) as being obvious on consideration of *Mori et al.* or *Kinzer.*

Mori et al. is directed to the structure of a power semiconductor device.

Kinzer is directed to a power transistor device having heavy metal doping.

Claim 9 is an independent claim and claims 10-14 depend from it. Claim 9 is directed to a semiconductor device which includes a substrate having region irradiated with radiating rays, crystal defects within the region irradiated, and a metal wiring layer located over the substrate. The metal wiring layer is made of a light metal. The metal wiring layer has an opening above the region irradiated so that radiating rays passing to the region irradiated through the opening generate the crystal defects within the region irradiated.

Claim 9 requires structure such that a metal wiring layer of a light metal is located over the substrate so as to have an opening above a region irradiated with radiating rays which cause crystal defects within the region irradiated. Neither *Mori* nor *Kinzer* discloses such structure. *Mori* discloses the structure of a power semiconductor, but does not disclose a light metal wiring layer having an opening over a region irradiated with radiating rays that have caused crystal defects within the region irradiated. Likewise, *Kinzer* discloses the structure and manufacturing method of a power transistor device which includes implanting heavy metals through windows. *Kinzer,* however, does not disclose a light metal wiring layer located over the substrate which has an opening over a region irradiated with radiating rays such that the radiating rays cause crystal defects within the region irradiated. The references do not point to the structure claimed in claim 9. Hence, claim 9 does not follow from and is nonobvious over the cited references. Claims 10-14 depend from claim 9 and further definite it. They are also patentable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

In view of the above, it is submitted that the application is in condition for allowance. Reconsideration and reexamination are requested. Allowance of claims 9-14 at an early date is solicited.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

The title has been changed as follows:

SEMICONDUCTOR DEVICE [AND A METHOD FOR MANUFACTURING THEREOF] WITH METAL WIRE LAYER MASKING

Paragraph beginning at line 18 of page 1 has been amended as follows:

A substrate 82 used for the IGBT 80 includes a drain layer 3 with P^+ type, an n^+ type layer 5 and an n^- type layer 7. Base regions 21 are formed in the n^- type layer 7, and source regions 23 with n^+ type are formed within the base regions 21. The s[S]urface of the n^- type semiconductor layer 82 is covered with a gate oxidation layer [17] 22.

Paragraph beginning at line 25 of page 1, has been amended as follows:

Incidentally, a loss caused by switching arises as a result of a parasitic diode generated on a plane of a PN (positive-negative) junction 59. Japanese Patent laid-open publication No. Hei 7-135214 discloses a technology for selectively radiating electron-beams using a mask 41 shown in Fig. 9 during the manufacturing processes in order to avoid the generation of the parasitic diode. The beams pass through through-holes 43 formed in the mask 41 and irradiate[d] on the IGBT 80. In this way, the life-time of carriers located on the plane of the PN junction 59 where the parasitic diode being generated can be shortened as a result of forming crystal defects 61.

Paragraph beginning at line 13 of page 2 has been amended as follows:

In the manufacturing processes described above, unexpected variation of the threshold voltage in the IGBT [9]80 is [pointed out] possible because of generation of bremsstrahlung caused by the material of the mask 41 made generally of a heavy metal such as lead and the like.

Paragraph beginning at line 18 of page 2 has been amended as follows:

Japanese Patent laid-open publication No. Hei 8-227895 discloses another IGBT 90 having layers for restricting electron-beams. As shown in Fig. 10, a layer 69 [for restricting the beams] made of silicon nitride for restricting the beams is formed under a source electrode [where requiring restriction of the electron-beams]. Generation of [the] bremsstrahlung is restricted even when the beams are radiated to the IGBT 90 [under the condition] due to masking [of] by the restriction layer 69.

Paragraph beginning at line 1 of page 3 has been amended as follows:

However, the number of processes is increased because the processes for forming the restriction layers 69 made of silicon nitride is required in the conventional method.

Paragraph beginning at line 6 of page 3 has been amended as follows:

It is an object of the present invention to overcome the above mentioned drawbacks associated with the prior art[s], and to provide a semiconductor device and a method for manufacturing thereof capable of radiating electron-beams to the desired region with simple processes, while not providing adverse effects caused by bremsstrahlung even when the electron-beams are radiated.

Paragraph beginning at line 13, page 3 has been amended as follows:

In accordance with characteristics of the present invention, there is provided a semiconductor device [comprises] comprising:

Paragraph beginning at line 18 of page 3 has been amended as follows:

a metal [wring] wiring layer located on the substrate one of directly and indirectly,

Paragraph beginning at line 20 of page 3 has been amended as follows:

wherein the metal [wring] wiring layer is made of a light metal,

paragraph beginning at line 22 of page 3 has been amended as follows:

and wherein the metal [wring] wiring layer located on the region to be irradiated is formed thinner than that formed on regions except for the region to be irradiated.

Paragraph beginning at line 25 of page 3 has been amended as follows:

Also, in accordance with characteristics of the present invention, there is provided a semiconductor device [comprises] comprising:

Paragraph beginning at line 4 of page 4 has been amended as follows:

a metal [wring] wiring layer located on the substrate,

Paragraph beginning at line 5 of page 4 has been amended as follows:

wherein the metal [wring] wiring layer is made of a light metal,

Paragraph beginning at line 7 of page 4 has been amended as follows:

and the metal [wring] wiring layer is used as a mask for restricting penetration of the radiating rays into regions except for the region to be irradiated.

Paragraph beginning at line 11 of page 5 has been amended as follows:

Fig. 5A and Fig. 5B are [an]other sectional views showing the manufacturing process of the IGBT 1.

Paragraph beginning at line 13 of page 5 has been amended as follows:

Fig. 6A and Fig. 6B are [far another] yet other sectional views showing the manufacturing process of the IGBT 1.

Paragraph beginning at line 15 of page 5 has been amended as follows:

Fig. 7A and Fig. 7B are still [an]other sectional views showing the manufacturing process of the IGBT 1.

Paragraph beginning at line 4 of page 6 has been amended as follows:

The IGBT 1 is formed on a substrate 2 for a semiconductor device. In the substrate 2, an n^+ type layer 5 and an n^- type layer 7 are consecutively formed on a drain layer 3 with P^+ type. A base region 21 with P^+ type is formed in the n^- type layer 7. Source regions 23 are formed in the base region 21. The surface of the n^- type layer 7 is covered with a gate oxidation layer 15. A gate electrode 17 is formed on the gate oxidation layer 15. The gate electrode 17 is covered with an inter-insulating layer 19, and a source electrode 22 made of aluminum is formed on the inter-insulating layer 19. The source electrode 22 formed as a wiring layer made of a metal is also used for electrically connecting with the source regions 23 in the IGBT element. A passivation layer 29 covers the entire surface of the source electrode 22. The first conductive type and the second conductive type are respectively defined as n type and p type in this embodiment.

Paragraph beginning at line 22 of page 6 has been amended as follows:

A silicon oxidation layer 27 is formed on a region 24 located between the source regions 23 formed within the base regions 21. Further, the source electrode 22 is not [existed] present at an upper part of the silicon oxidation layer 27, and an opening 25 is located on the silicon oxidation layer 27. On the other hand, a crystal defect region 11 is formed at a position in the n^- type layer 7 and below the silicon oxidation layers 27.

Paragraph beginning at line 4 of page 7 has been amended as follows:

Fig. 2 is a perspective view of the IGBT 1 before forming the passivation layer 29. As described, the silicon oxidation layer 27 is formed above [of] the crystal defect region 11, and the opening 25 is located on the silicon oxidation layers 27. In this way, the source electrode 22 made of aluminum can be used both for a wiring, and a mask for the beams.

Paragraph beginning at line 11 of page 7 has been amended as follows:

Next, a method for manufacturing the IGBT 1 will be described. The manufacturing processes similar to an ordinary IGBT are carried out until forming the source electrodes 23. In other words, the substrate 2 is formed by consecutively forming the n^+ type layer 5 on the drain layer 3 and the n^- type layer 7 thereon as shown in Fig. 4A. Thereafter, the gate oxidation layer 15 and the gate electrode 17 are formed successively as shown in Fig. 4B. Ion implantation of P-type impurities is carried out by using the gate electrode 17 as a mask. Further, N-type

impurities are implanted ionically by using both [a] resist layers 81 formed on the gate oxidation layer 15 and the gate oxidation layers 17 as a mask as shown in Fig. 4C. The base region 21 with P^+ type and a pair of the source regions 23 located in the base region 21 are formed simultaneously by carrying out thermal treatment as shown in Fig. 5A.

Paragraph beginning at line 2 of page 8 has been amended as follows:

Next, a silicon oxidation (SiO_2) layer 18 is accumulated entirely on the substrate with the chemical vapor deposition (CVD) method as shown in Fig. 5B. A resist layer 82 is formed above [of] both the crystal defect region 11 and the gate electrode 17 as shown in Fig. 6A. Both the inter-insulation layer 19 and the silicon oxidation layer 27 are formed with an etch-back technique by using the resist layers 82. In this way, the silicon oxidation layer 27 is formed above of the crystal defect region 11 as shown in Fig. 6B.

Paragraph beginning at line 24 of page 8 has been amended as follows:

By carrying out the irradiation, the crystal defect region 11 uncovered with the source electrode 22 is irradiated by the beams, so that desired crystal defects are generated within the region 11. On the other hand, less [amount] intensity of the beams are irradiated to regions existing outside of the region 11. Although, a certain amount[s] of crystal defects are generated in the regions existing [the] outside of the region 11, these defects can be removed by annealing carried out later. In this way, the IGBT 1 shown in Fig. 1 is manufactured.

Paragraph beginning at line 8 of page 9 has been amended as follows:

Next, thickness of the source electrode 22 is described hereunder with reference to a relationship between a range of electrons in the source electrode 22 and energy amount of the beams. As shown in Fig. 3, the range of electrons in aluminum is increased when a higher energy is radiated. Usually, energy strength of the beams forming the crystal defect region is in a range from 600 electro-volts to 1 mega electro-volts. The source electrode 22 in thickness of 0.6 cm to 1 cm is required in order to restrict the generation of the crystal defect region with the source electrode 22 alone. However, the source electrode, 22 relatively thicker than an ordinary aluminum wiring having a range from 1 μm to 10 μm, is able to restrict the beams because the

beams are restricted by the gate electrode 17, the passivation layer 19 and other layers formed thereunder.

Paragraph beginning at line 24 of page 9 has been amended as follows:

Further, the generation of [the] bremsstrahlung caused by the source electrode 22 made of a heavy metal can be avoided even when the beams are directly radiated to the source electrode 22 exposed to the air. Because the source electrode 22 is made of a light metal in this embodiment. In this way, only a desired region [can be] is irradiated with [the] beams by using the source electrode made of aluminum capable of [using] being used both as a wiring and a mask for the beams as a result of making an opening at a region to be irradiated without forming a layer for restricting beams in addition to the layers described above

Paragraph beginning at line 22 of page 10 has been amended as follows:

Although, the source electrode 22 is made of aluminum, other light metals not causing bremsstrahlung such as an aluminum silicon and the like can be used for the source electrode 22. Any other metals not causing bremsstrahlung such as copper can be used for the source electrode 22. Because of its higher density than that of aluminum, the use of copper allows [the] radiation of the beams to the desired region even when its profile is in a thin form. Further, tungsten can also be used for the source electrode 22.

Paragraph beginning at line 10 of page 11 has been amended as follows:

Further, the silicon oxidation layer 27 is provided in order to form the opening 25 located above [of] the crystal defect region 11 in the embodiment. However, the opening can be formed directly on the source electrode 22 by carrying out etching thereto without providing the silicon oxidation layer.

Paragraph beginning at line 16 of page 11 has been amended as follows:

The semiconductor device in accordance with the present invention is characterized in that, the metal [wring] wiring layer is made of a light metal. Therefore, no generation of [the] bremsstrahlung is observed even when the radiation [are] is radiated. Also, the metal [wring] wiring layer located on the region to be irradiated is formed thinner than that formed on regions

except for the region to be irradiated so as to reach the radiating rays to the region to be irradiated. In this way, the crystal defect region can only be formed in the desired region. As a result, it is possible to provide a semiconductor device capable of radiating the radiating rays to the desired region with simple processes, while not providing adverse effects caused by bremsstrahlung even when the radiating rays are radiated. Also, the semiconductor device in accordance with the present invention is characterized in that, the metal [wring] wiring layer located on the regions except for the region to be irradiated is formed in a thickness so as not to provide any adverse effect on the regions except for the region to be irradiated. Therefore, it is possible to avoid adverse effect on the regions except for the region to be irradiated.

Paragraph beginning at line 12 of page 12 has been amended as follows:

Further, the semiconductor device in accordance with the present invention is characterized in that, the metal [wring] wiring layer is made of a light metal, and the metal [wring] wiring layer is used as a mask for restricting penetration of the radiating rays into region except for the region to be irradiated. Therefore, it is possible to provide a semiconductor device capable of [radiating] receiving the radiating rays only to the desired region with simple processes, while not providing the adverse effects caused by bremsstrahlung even when the radiating rays are radiated.

Paragraph beginning at line 12 of page 13 has been amended as follows:

Further, the method for manufacturing a semiconductor device in accordance with the present invention is characterized in that, the method comprises the steps of entirely forming the metal wiring layer, removing the metal wiring layer located on the region to be irradiated, and radiating the radiating rays using the metal wiring layer [being remained] remaining as a mask. Therefore, it is possible to provide a semiconductor device capable of radiating the radiating rays only to the desired region with simple processes without causing any adverse effects caused by [the] bremsstrahlung even when the radiating rays are radiated.

Paragraph beginning at line 24 of page 13 has been amended as follows:

The semiconductor device in accordance with the present invention is characterized in that, the metal wiring layer is made of a metal which prevents the generation of [the]

bremsstrahlung even when the radiating rays are radiated, and the metal [wring] wiring layer located on the region to be irradiated is formed thinner than that formed on regions except for the region to be irradiated so as to reach the radiating rays to the region to be irradiated. In this way, the crystal defect region can only be formed in the desired region. As a result, it is possible to provide a semiconductor device capable of radiating the radiating rays only to the desired region with simple processes, while not providing adverse effects caused by [the] bremsstrahlung even when the radiating rays are radiated.

In the Claims

Please cancel claims 1-8, without prejudice. Claims 1-7 have been rewritten as the new claims. Claim 8 has been withdrawn as being directed to a non-elected invention and a divisional application may be filed.

Please add claims 9-14, as follows:

9. (New) A semiconductor device comprising:

a substrate having a region irradiated with radiating rays,

crystal defects within the region irradiated, and

a metal wiring layer located over the substrate, the metal wiring layer being made of a light metal, the metal wiring layer having an opening above the region irradiated, so that radiating rays passing to the region irradiated through the opening generate the crystal defects within the region irradiated.

10. (New) The semiconductor device in accordance with Claim 9, wherein the metal wiring layer is formed in a thickness so as to restrict penetration of the radiating rays into the region irradiated.

11. (New) The semiconductor device in accordance with Claim 10, wherein an insulating layer is formed above the region irradiated, the opening being on the insulating layer.

12. (New) The semiconductor device in accordance with Claim 11, wherein the metal wiring layer covers a part of the insulating layer.

13. (New) The semiconductor device in accordance with Claim 12, wherein the semiconductor device is an insulated gate bipolar transistor, and wherein the region irradiated is a positive-negative junction where a parasitic diode is generated.

14. (New) The semiconductor device in accordance with Claim 12, wherein the semiconductor device is a metal oxide semiconductor field effect transistor, and wherein the region irradiated is a positive-negative junction region where a parasitic diode is generated.

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